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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,559	12/29/2003	Justin K. Brask	P18244	9088

7590 08/04/2005

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,559	BRASK ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-16* is/are allowed.

6)☒ Claim(s) *9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20 June 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 20 June 2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6303418 to Cha et al. in view of US 6835639 to Rotondaro et al.

Regarding claim 9, Cha discloses a method for making a semiconductor device in fig. 1-9 comprising: forming a first polysilicon layer 17, column 4 line 63, which is bracketed by a pair of sidewall spacer 9, column 4 line 52, on a first gate dielectric layer 16, column 4 line 55, and polysilicon layer 17 on a second gate dielectric layer 16, fig. 6; removing the first polysilicon layer 17 to generate a trench 15 that is positioned between the pair of sidewall spacers 9, fig. 7; forming an n-type metal layer 19, column 5 line 21 within the trench.

But Cha does not disclose the method comprising a p-type polysilicon layer on a second gate dielectric and converting substantially all of p-type polysilicon layer to a silicide.

However, Rotondaro discloses the method converting substantially all of the PMOS polysilicon layer (si), column 3 lines 6 and 59, fig. 2, to a silicide, column 3 line 26, fig. 7. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the PMOS silicide gate teaching of Rotondaro with Cha's method, because it would have created a CMOS having PMOS gate electrode with different work function as taught by Rotondaro, see abstract.

Regarding claim 10, Cha discloses the method wherein the first gate dielectric layer 16 and the second gate dielectric layer 16 each comprise high k or nitride oxide, column 4 line 54, and wherein the first polysilicon layer 17 and the polysilicon layer 17 are each between about 200 and about 5,000 angstroms thick, column 5 lines 58 and 65.

But Cha does not discloses the gate first gate dielectric layer and the second gate dielectric layer each comprise silicon dioxide,

However, Rotondaro discloses the method wherein the first gate dielectric layer and the second gate dielectric layer each comprise silicon dioxide or high k, column 3 line 14, and wherein the first polysilicon layer and the p-type polysilicon layer are each between about 1000 angstroms thick, column 3 line 59. Accordingly, it would have been obvious to one of ordinary skill in art to use the gate dielectric thickness teaching of Rotondaro with Chas's method in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

With respect to silicon dioxide, At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use teaching of Rotondaro with Chas's method, because such material substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06

Regarding claim 11, Cha discloses the method wherein a wet etch process that is selective for the first polysilicon layer over the p-type polysilicon layer is applied to remove the first polysilicon layer, column 5 line 9-10.

Regarding claim 12, Cha discloses the method wherein the N-type metal layer comprising a material that is selected from the group consisting of hafnium, zirconium, tantalum, aluminum, and metal carbide, column 5 line 21

But, Cha does not disclose the method wherein all of the p-type polysilicon layer is converted to a silicide.

However, Rotondaro discloses the method converting substantially all of the PMOS polysilicon layer, column 3 line 59 fig. 2, to a silicide, column 3 line 26. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the PMOS silicide gate teaching of Rotondaro with Cha's method, because it would have created a CMOS with different work function as taught by Rotondaro, see abstract.

5. Claim 9 rejected under 35 U.S.C. 103(a) as being obvious over US 6770568 to Brask in view of US 6835639 to Rotondaro et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject

matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 9, Brask discloses a method for making a semiconductor device in fig. 1-3 comprising: forming a first polysilicon layer 14, column 2 line 34, which is bracketed by a pair of sidewall spacer16, column 2 line 24, on a first gate dielectric layer 13, column 2 line 24, and P-type polysilicon layer 14 (PMOS) on a second gate dielectric layer 13, fig. 1; removing the first polysilicon layer 14 to generate a trench 20a, fig. 2, that is positioned between the pair of sidewall spacers 16, fig. 2; forming an n-type metal layer 15, column 2 line 60, within the trench, fig. 3.

But Brask does not disclose the method converting substantially all of p-type polysilicon layer to a silicide.

However, Rotondaro discloses the method converting substantially all of the PMOS polysilicon layer (si), column 3 lines 6 and 59, fig. 2, to a silicide, column 3 line 26, fig. 7. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the PMOS silicide gate teaching of Rotondaro with Brask's method, because it would have created a CMOS

having PMOS gate electrode with different work function as taught by Rotondaro, see abstract.

Allowable Subject Matter

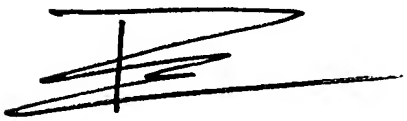
6. Claims 13-16 are allowed because the because the prior art of record neither anticipated nor rendered obvious all the limitations of the base claim 13 including remove the n-type polysilicon layer without removing significant portion of the p-type polysilicon layer, exposing the first gate dielectric layer; removing the exposed first gate dielectric layer; forming a high-k gate dielectric layer on the substrate at the bottom of the trench, forming an n-type metal layer on the high-k dielectric layer.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
Patent Examiner
01 Aug. 2005